What is claimed is:

1. A data conversion/output apparatus comprising:

a large number of sensors;

voltage-time conversion circuits which are arranged adjacent to said respective sensors and change output levels upon the lapse of times corresponding to output voltage values from said sensors after a conversion operation start point in order to convert voltage outputs of said sensors into times; and

sensed data generation circuits for outputting, as digital data, lapse times until the output levels of said voltage-time conversion circuits change after a substantial conversion start point.

2. An apparatus according to claim 1, further comprising control means for sequentially supplying outputs from said voltage-time conversion circuits to said sensed data generation circuits.

3. An apparatus according to claim 1, wherein

said sensors are arranged in a matrix together with said corresponding voltage-time conversion circuits to constitute respective pixels, and

said data conversion/output apparatus further comprises group selection means for selecting, from the pixels in a column direction, pixels which are aligned

in a row direction and connected to one of said sensed data generation circuits.

4. An apparatus according to claim 3, wherein said sensed data generation circuit includes a counter for counting a clock signal, and a latch circuit for latching a count value after the conversion operation start point of said counter upon reception of an output from said voltage-time conversion circuit of each group-selected pixel.

5. An apparatus according to claim 3, wherein said sensed data generation circuit includes a counter for counting a clock signal, and a gate circuit for controlling count of the clock signal from said counter until an output from said voltage-time conversion circuit of each group-selected pixel is obtained after the conversion operation start point.

6. An apparatus according to claim 3, wherein said sensed data generation circuit includes a counter for counting a clock signal, a first latch circuit for latching a count value of said counter upon reception of an output from said voltage-time conversion circuit of each pixel in a selected group, and a second latch circuit for latching an output from said latch circuit.

7. An apparatus according to claim 6, wherein an output from said second latch circuit is output as sensed data upon reception of a signal designating an individual pixel of the selected group.

8. An apparatus according to claim 3, wherein said sensed data generation circuit includes a counter for counting a clock signal, and a latch circuit for latching a count value of said counter upon reception of an output from said voltage-time conversion circuit of each group-selected pixel, and said latch circuit is arranged in each pixel.

9. An apparatus according to claim 3, wherein said sensed data generation circuit includes a counter for counting a clock signal, and a latch circuit for latching a count value of said counter after the conversion operation start point upon reception of an output from said voltage-time conversion circuit of each pixel, and said sensed data generation circuit is arranged in each pixel.

10. An apparatus according to claim 3, wherein said sensed data generation circuit includes a counter for counting a clock signal, and a gate circuit for controlling count of the clock signal from said

counter until an output from said voltage-time conversion circuit is obtained after the conversion operation start point, and

said sensed data generation circuit is arranged in each pixel.

11. An apparatus according to claim 3, wherein said sensed data generation circuit includes a counter for counting a clock signal, and a latch circuit for latching a count value of said counter after a point offset from the conversion operation start point upon reception of an output from said voltage-time conversion circuit of each group-selected pixel.

12. An apparatus according to claim 3, wherein said sensed data generation circuit includes a counter for counting a clock signal, and a gate circuit for controlling count of the clock signal from said counter until an output from said voltage-time conversion circuit of each group-selected pixel is obtained after a time point offset from the conversion operation start point.

13. An apparatus according to claim 3, wherein said sensed data generation circuit includes a counter for counting a clock signal, and a latch circuit for latching a count value of said counter after a time

point offset from the conversion operation start point upon reception of an output from said voltage-time conversion circuit, and

said latch circuit is arranged in each pixel.

14. An apparatus according to claim 3, wherein

said sensed data generation circuit includes a counter for counting a clock signal, and a gate circuit for controlling count of the clock signal until an output from said voltage-time conversion circuit is obtained after a time point offset from the conversion operation start point, and

said sensed data generation circuit is arranged in each pixel.

15. An apparatus according to claim 3, wherein said sensed data generation circuit includes a counter for counting a clock signal for generating digital data corresponding to the output level of said voltage-time conversion circuit, and a count control circuit for controlling a count operation speed of said counter.

16. An apparatus according to claim 3, wherein said sensed data generation circuit includes means for changing a clock frequency of a clock signal.

17. A data conversion/output apparatus comprising:

a column decoder for selecting at once a plurality of pixels aligned on an arbitrary column from pixels arrayed in a matrix;

a plurality of data buses each commonly connected to a plurality of pixels aligned on each row out of the pixels;

a counter for sequentially outputting count values in accordance with internal count operation;

a plurality of latch circuits which are arranged on respective rows and latch the count values from said counter in accordance with level changes of said data buses corresponding to the respective rows;

a row decoder for selecting a row having a desired pixel out of the pixels selected by said column decoder; and

a plurality of row switches which are arranged on the respective rows and output as sensed data of desired pixels the count values latched by said latch circuits corresponding to the respective rows,

wherein each of the pixels has

a sensor for outputting a detection result as an output voltage value,

a voltage-time conversion circuit for changing an output level upon the lapse of time corresponding to an output voltage value from said sensor after a predetermined conversion operation start point, and

a column switch for outputting in accordance

with selection of a pixel by said row decoder an output from said voltage-time conversion circuit to a data bus connected to the pixel.

18. An apparatus according to claim 17, further comprising a plurality of output-side latch circuits which are interposed between said latch circuits and said row switches for the respective rows, latch outputs from said latch circuits in accordance with a predetermined data reception signal, and output the outputs to said switches.

19. A data conversion/output apparatus comprising:

a column decoder for selecting at once a plurality of pixels aligned on an arbitrary column from pixels arrayed in a matrix;

a plurality of data buses each commonly connected to a plurality of pixels aligned on each row out of the pixels;

a clock generation circuit for outputting a clock signal having a predetermined frequency;

a plurality of row counters which are arranged on respective rows, count clock signals from said clock generation circuit, and output count values to row switches;

gate circuits which are arranged on the respective rows and control output of the clock signals

from said clock generation circuit to said row counters on the basis of output levels of said data buses;

a row decoder for selecting a row having a desired pixel out of the pixels selected by said column decoder; and

a plurality of row switches which are arranged on the respective rows and output as sensed data of desired pixels the count values from said row counters corresponding to the respective rows,

wherein each of the pixels has

a sensor for outputting a detection result as an output voltage value,

a voltage-time conversion circuit for changing an output level upon the lapse of time corresponding to an output voltage value from said sensor after a predetermined conversion operation start point, and

a column switch for outputting in accordance with selection of a pixel by said row decoder an output from said voltage-time conversion circuit to a data bus connected to the pixel.

20. An apparatus according to claim 19, further comprising a plurality of output-side latch circuits which are interposed between said row counters and said row switches for the respective rows, latch outputs from said row counters in accordance with a predetermined data reception signal, and output the outputs to said

switches.